MC68HC811E2 DEVICE INFORMATION
B19C Mask Set

The following information is presented to users of MC68HC811E2 samples from the B19C mask set.

USER INFORMATION:

This information sheet is to be used as a supplement to the MC68HC811A2 Technical Summary. A new data sheet for the MC68HC11E9 is now available. It can be used for additional information regarding Port and Timer changes, Block Protect, and Internal Read Visibility.

Current samples of the 68HC811E2 are being tested at 250C and 850C.

ERRATA:

Use of slow edges on signals feeding the the timer input capture or pulse accumulator inputs is not recommended. Use of buffers with edges faster than 100 nsec will prevent system noise generating false captures. In conjunction with faster edges, we have re-specified the timer input pulse width to be slightly longer than a system clock period to properly capture transitions. See section 11 of the MC68HC11E9 data sheet for details.

The CPU will not exit STOP mode correctly when interrupted by IRQ or XIRQ if the instruction immediately preceding STOP is a column 4 or 5 accumulator inherent (opcodes $4X and $5X) instruction, such as NEGA, NEGB, COMA, COMB, etc. These single byte, two cycle instructions must be followed by a NOP, then the STOP command. If reset is used to exit STOP mode, the CPU will respond correctly.

In the gated time accumulation mode, multiple transitions on the PAI input may cause extra counts due to a race in the Pulse Accumulator circuit.

Initial samples of the B19C mask have high RAM standby current. The RAM works properly in all modes, however, in power-down mode, the standby current may exceed 5005A.

The peripheral data write delay time (tPWD) for Ports A, B, C, and D can exceed data sheet limits at high temperature. Motorola will be changing the specification for these ports to the following:

Port A tPWD: 200ns All frequencies and temperatures.

Ports B, C, & D tPWD: 1/4tcyc + 100ns All frequencies and temperatures.

68HC811E2 FUNCTIONAL FEATURE CHANGES

PORT DIFFERENCES:

On the 68HC811A2, bit 3 of port A is an output only pin which is driven low in reset. When used as an ordinary port output, the state of the pin can be changed by writing to the port A data register. Either of the timer output compare functions (OC1 or OC5) can be enabled at PA3 by writing to the appropriate timer control bits.

On the 68HC811E2, PA3 is bidirectional. It is an input in reset and will remain so until either the new data direction bit (DDRA3) is changed or an output compare is enabled. If the pin is to be used as a port output, DDRA3 must first be written to a one. The pin can also be enabled for either OC1, OC5, or IC4. Since the state of the DDRA3 bit does not affect the functioning of the pin as an output compare, no software change is required in upgrading from a 68HC811A2 to a 68HC811E2 if PA3 is already used for either OC1 or OC5. A software (and possibly hardware) change is required if PA3 is used as a general port ouptut.

FOURTH INPUT CAPTURE:

The functionality of the 68HC811E2 timer was upgraded by modifying the function of the fifth output compare feature similar to that of the 68HC11E9. This timer channel, associated with port A, bit 3, is now software selectable as either input capture 4 or as output compare 5 (the default setting). Bit 2 (I4/O5) of the PACTL register is now used to distinguish between the IC4 and OC5 features. Setting this bit to 0 enables OC5, and to one enables IC4. Bit 3 (DDRA3) of the PACTL register now becomes the data direction register bit associated with port A, bit 3. For input functions this bit must be 0 (default or reset value), and for output functions, one.

The TI4O5 register (16 bits), the interrupt enable control bit (I4O5I), and the interupt flag bit (I4O5F) will be shared by both functions, but operation of these registers and bits is dependent on whether the input capture or ouput compare function is being performed. The EDG4A and EDG4B control bits have been added to specify which edge(s) will be detected when input capture 4 is selected. These new bits now reside in the TCTL2 register as bits 6 and 7 respectively. For more detailed descriptions of the control registers and bits involved, see the timer chapter (Section 8) of the MC68HC11E9 data sheet.

BLOCK PROTECT REGISTER:

A block protect register has been added to enhance the data security of the EEPROM and CONFIG register. This BPROT register has been added to the register bank at address $1035. It functions by disabling the appropriate row drivers in the EEPROM or the CONFIG register during programming and erasing. Any application that allows alteration of EEPROM or CONFIG will require a modification to the initialization (reset) routines to disable BPROT.

The 2K EEPROM on the XC68HC811E2 is divided into four sections: $F800 - $F9FF, $FA00 - $FBFF, $FC00 - $FDFF & $FE00 - $FFFF. Four bits of the BPROT register are associated with each of these sections: BPRT0, BPRT1, BPRT2 & BPRT3 respectively.

These bits are located as bits 0,1,2 & 3 of the BPROT register. Additionally, bit 4 of the BPROT register is associated with the CONFIG register at location $103F.

After reset, these bits in the BPROT register are set to one. This disables alteration of the CONFIG register or of any byte of EEPROM. These bits may independently be cleared to zero, enabling normal alteration of the EEPROM or CONFIG register, but only during the first 64 cycles after reset. The memory space may be re-secured at any time by writing the associated bit back to a one, but this may be done only once. A subsequent clearing of a bit may only be done by executing a reset sequence. Additional information regarding the block protection mechanism may be found in the 68HC11E9 data sheet.

INTERNAL READ VISIBILITY (IRV):

The IRV funtion of the 68HC811E2 was modified to enable internal read visibility during normal expanded mode operation. The IRV bit is normally used for debug in the special test mode to enable visibility of internal reads on the expansion data bus. IRV is writeable anytime in test mode and one time only between resets in normal expanded mode. If IRV is clear, visibility of internal reads is inhibited. If the bit is set, internal reads are visible on the external bus. The user must ensure that bus conflicts do not occur by disabling all external devices from driving the data bus during any internal access.

Register Differences

68HC811A2 68HC811E2 Description of Change

TOC5 TI4O5 Same register, now dual purpose

TCTL2 TCTL2 Bits 6 & 7 added for EDG4A & EDG4B

TMSK1 TMSK1 Bit 3 changed to I4O5I

TFLG1 TFLG1 Bit 3 changed to I4O5F

PACTL PACTL Bits 2 & 3 added for I4/O5 & DDR3

Reserved BPROT Block protect register added at $1035

HPRIO HPRIO IRV bit now writeable once in expanded mode

Revision 0.0, 20 NOV 96

last update: Mar 26 1998